IBM POWER8 CPU

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Outline

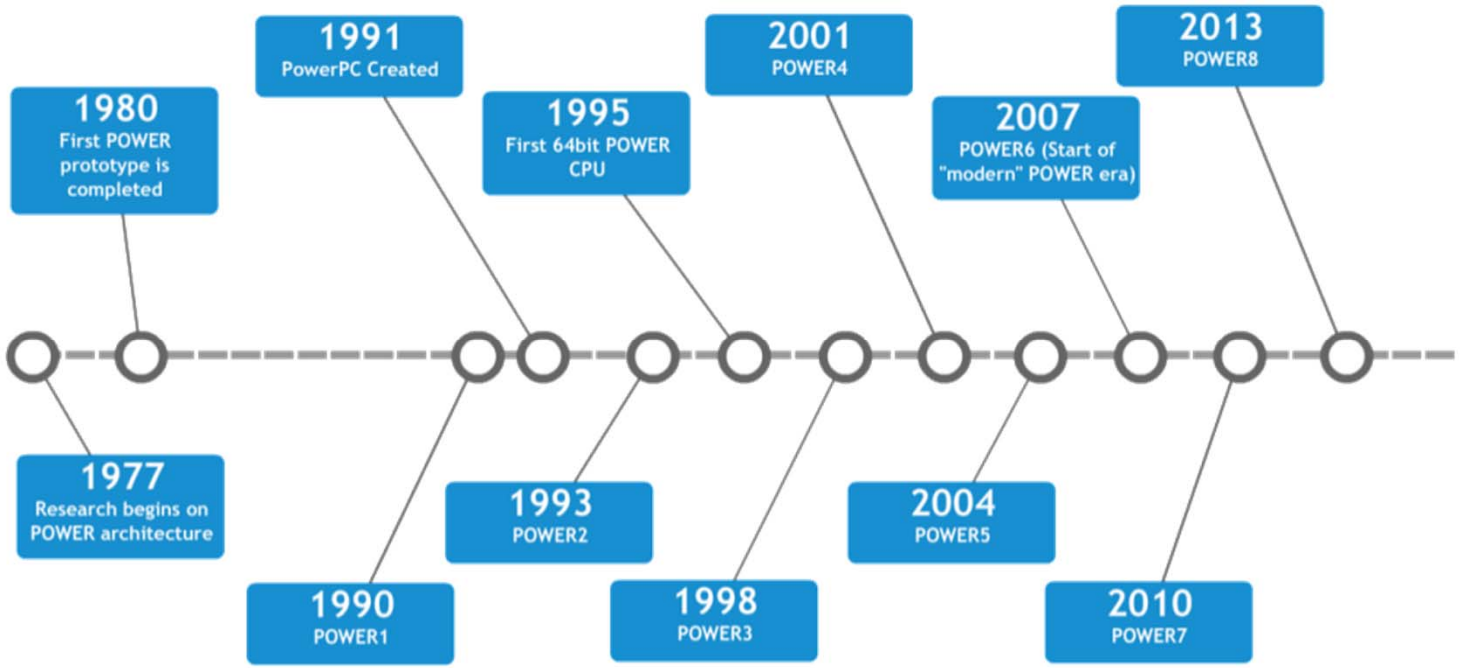
1. Background of POWER CPUs
2. POWER8
3. POWER8 vs POWER7
4. POWER vs other architectures
5. Future of POWER8

POWER Background

What is the POWER Architecture?

- RISC architecture developed by IBM
- Acronym for *Performance Optimization with Enhanced RISC*
- Not the same as POWER ISA (a deprecated IBM RISC architecture)
- Open for licensing

Timeline



Credit: readwritethink.org timeline generator

Goals of POWER8

- Compete with the x86 Architecture
- Focus on support for Linux machines
- Create an open-source processor, with the OpenPOWER Consortium
- Scalability
- Target servers/large systems, IBMi OS's, Linux

Implementations

- IBM's Watson (POWER7-8)
- Mars rovers (POWER1)
- Servers
- PowerPC (modified version of POWER architecture)

POWER8 Introduction

Specifications

- 12 cores, 8 SMT each
- 2.5 to 5 GHz clock speed
- 650 millimeters square
- Binary compatible with previous POWER versions
- On-board power management based on the PowerPC 405 CPU
- Direct Integration of PCIe 3

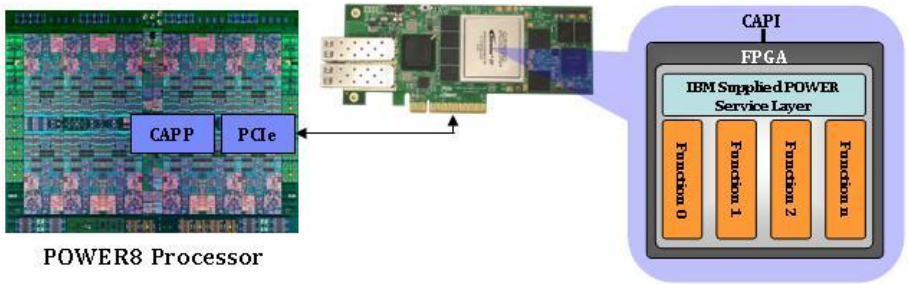
CAPI: Coherent Accelerator Processor Interface

- Allows direct communication between CPU and PCIe connected devices
- Removes OS and Driver overhead
- More coherent memory addressing
- Follows more natural programming model
- Accomplished by circumventing I/O bridge used in predecessor

Power Systems

IBM

Coherent Accelerator Processor Interface (CAPI) Overview



POWER8 Processor

Typical I/O Model Flow

DD Call → Copy or Pin Source Data → MMIO Notify Accelerator → Acceleration → Poll / Int Completion → Copy or Unpin Result Data → Ret. From DD Completion

Flow with a Coherent Model

Shared Mem. Notify Accelerator → Acceleration → Shared Memory Completion

Advantages of Coherent Attachment Over I/O Attachment

- Virtual Addressing & Data Caching
  - Shared Memory
  - Lower latency for highly referenced data
- Easier, Natural Programming Model
  - Traditional thread level programming
  - Long latency of I/O typically requires restructuring of application
- Enables Apps Not Possible on I/O
  - Pointer chasing, etc…

http://dancingdinosaur.wordpress.com/tag/coherent-accelerator-processor-interface-capi-power8/

Centaur

- Designed to be a generic memory controller
  - Memory can be upgraded from DDR3 to DDR4 when it is released
- Half L4 Cache, Half Controller
- Each POWER8 can have up to 8 Centaur Chips, 9.6 GB/s bandwidth per channel

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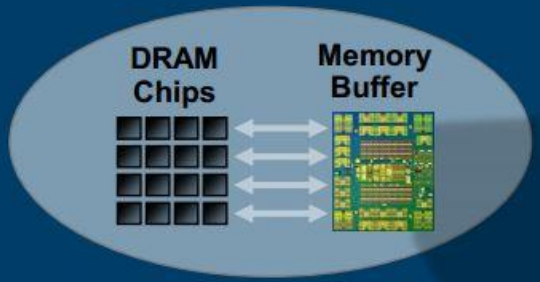
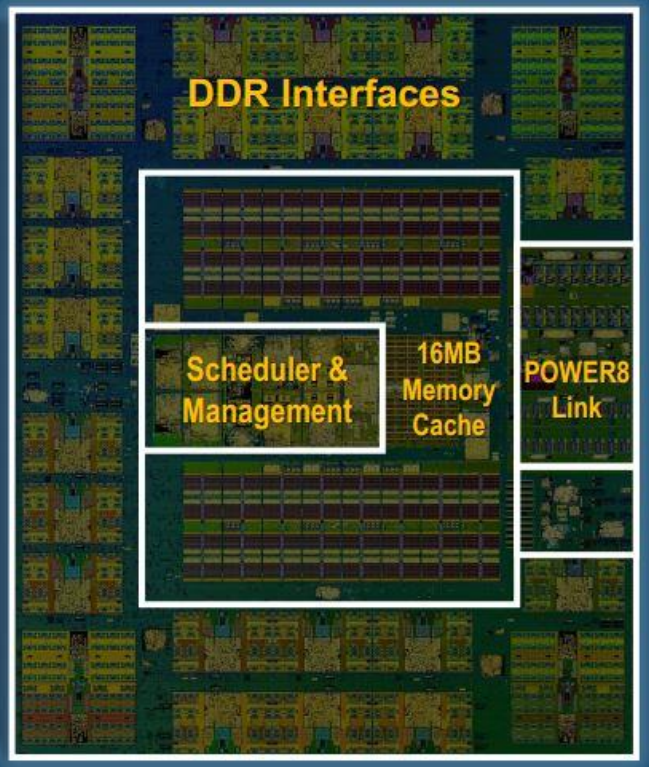
POWER8 Memory Buffer Chip *…with 16MB of Cache…*



Intelligence Moved into Memory
- Scheduling logic, caching structures
- Energy Mgmt, RAS decision point
  - Formerly on Processor
  - Moved to Memory Buffer

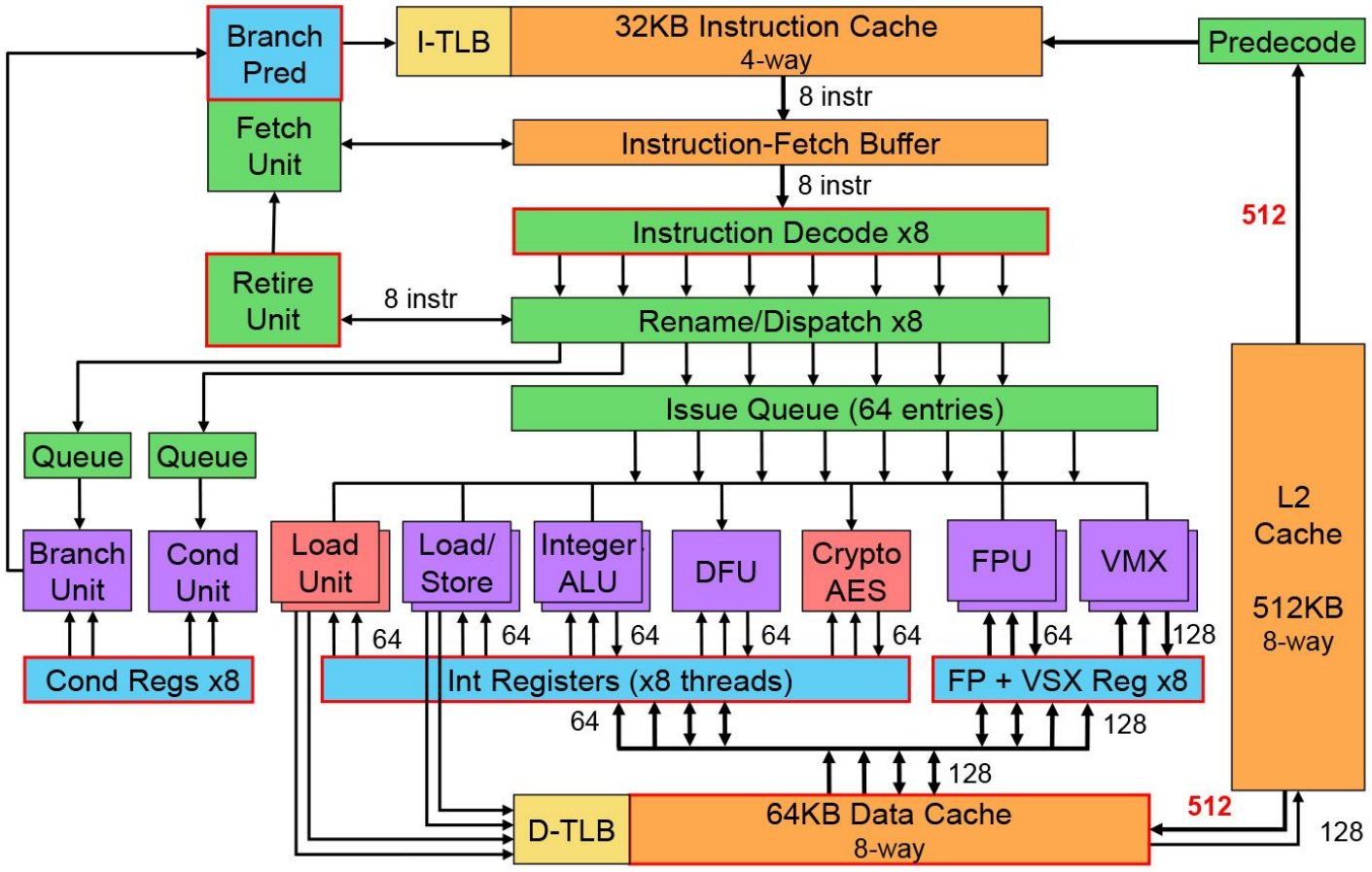
Processor Interface
- 9.6 GB/s high speed interface
- More robust RAS
- "On-the-fly" lane isolation/repair
- Extensible for innovation build-out

Performance Value
- End-to-end fastpath and data retry (latency)
- Cache → latency/bandwidth, partial updates
- Cache → write scheduling, prefetch, energy
- 22nm SOI for optimal performance / energy
- 15 metal levels (latency, bandwidth)



http://www.hotchips.org/wp-content/uploads/hc_archives/hc25/HC25.20-Processors1-epub/HC25.26.210-POWER-Studecheli-IBM.pdf

Pipeline



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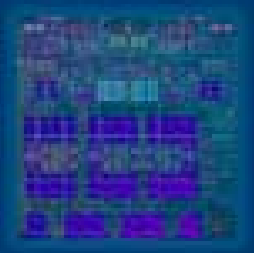
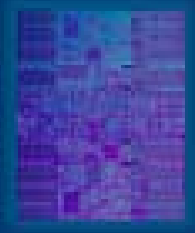
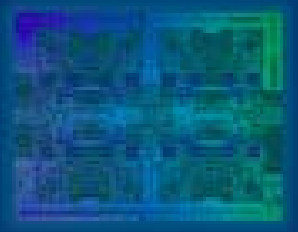
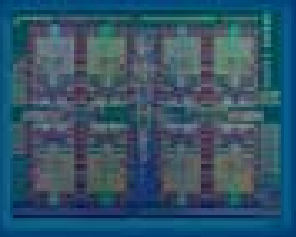
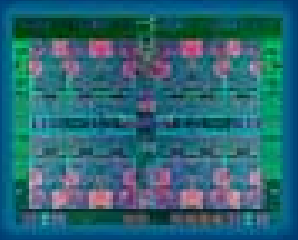
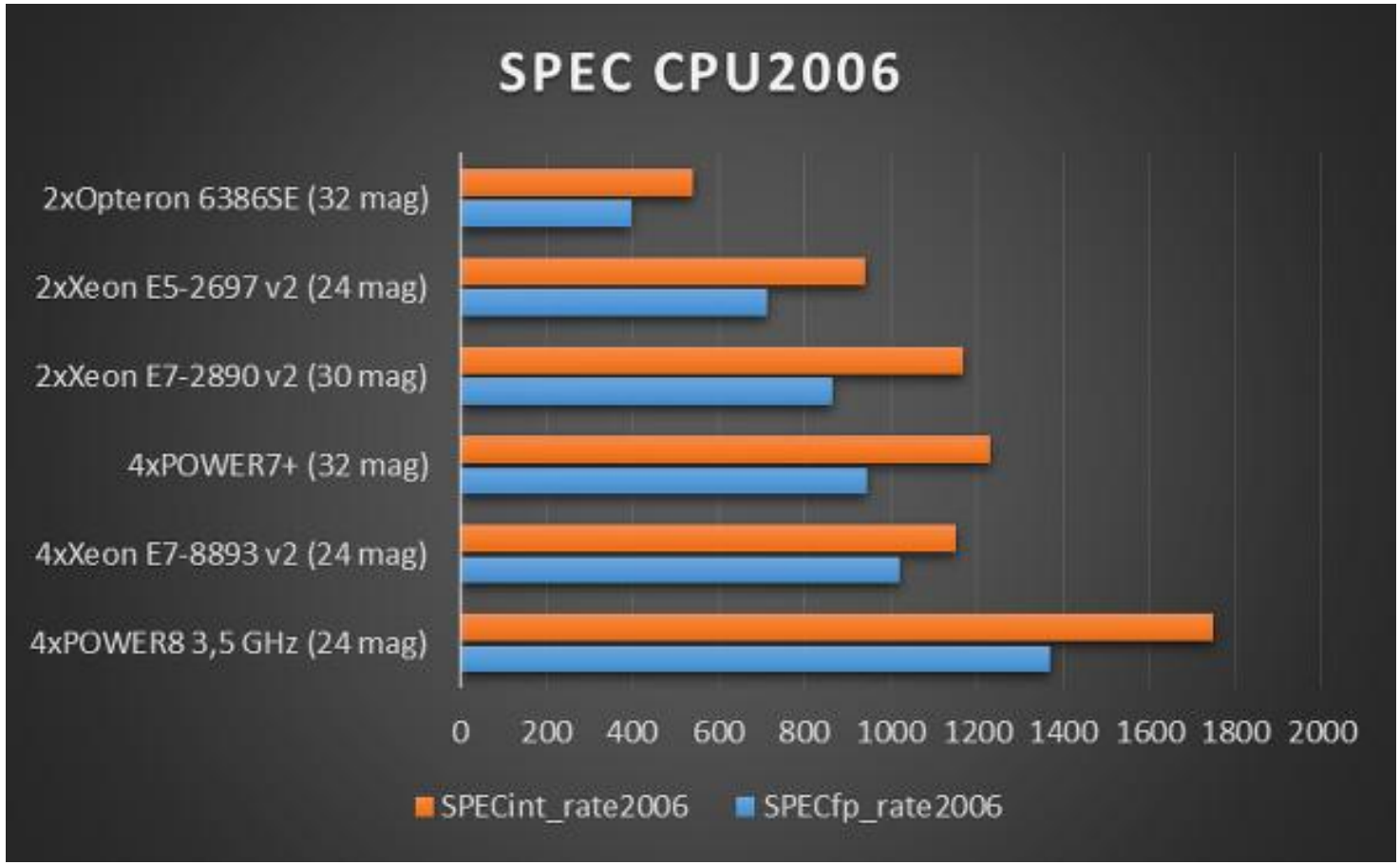
POWER8 Innovation

	POWER5 2004	POWER6 2007	POWER7 2010	POWER7+ 2012	POWER8
					
Technology	130nm SOI	65nm SOI	45nm SOI eDRAM	32nm SOI eDRAM	22nm SOI eDRAM
Compute					
Cores	2	2	8	8	12
Threads	SMT2	SMT2	SMT4	SMT4	SMT8
Caching					
On-chip	1.9MB	8MB	2 + 32MB	2 + 80MB	6 + 96MB
Off-chip	36MB	32MB	None	None	128MB
Bandwidth					
Sust. Mem.	15GB/s	30GB/s	100GB/s	100GB/s	230GB/s
Peak I/O	3GB/s	10GB/s	20GB/s	20GB/s	48GB/s

Comparison with Other Architectures

Benchmarks

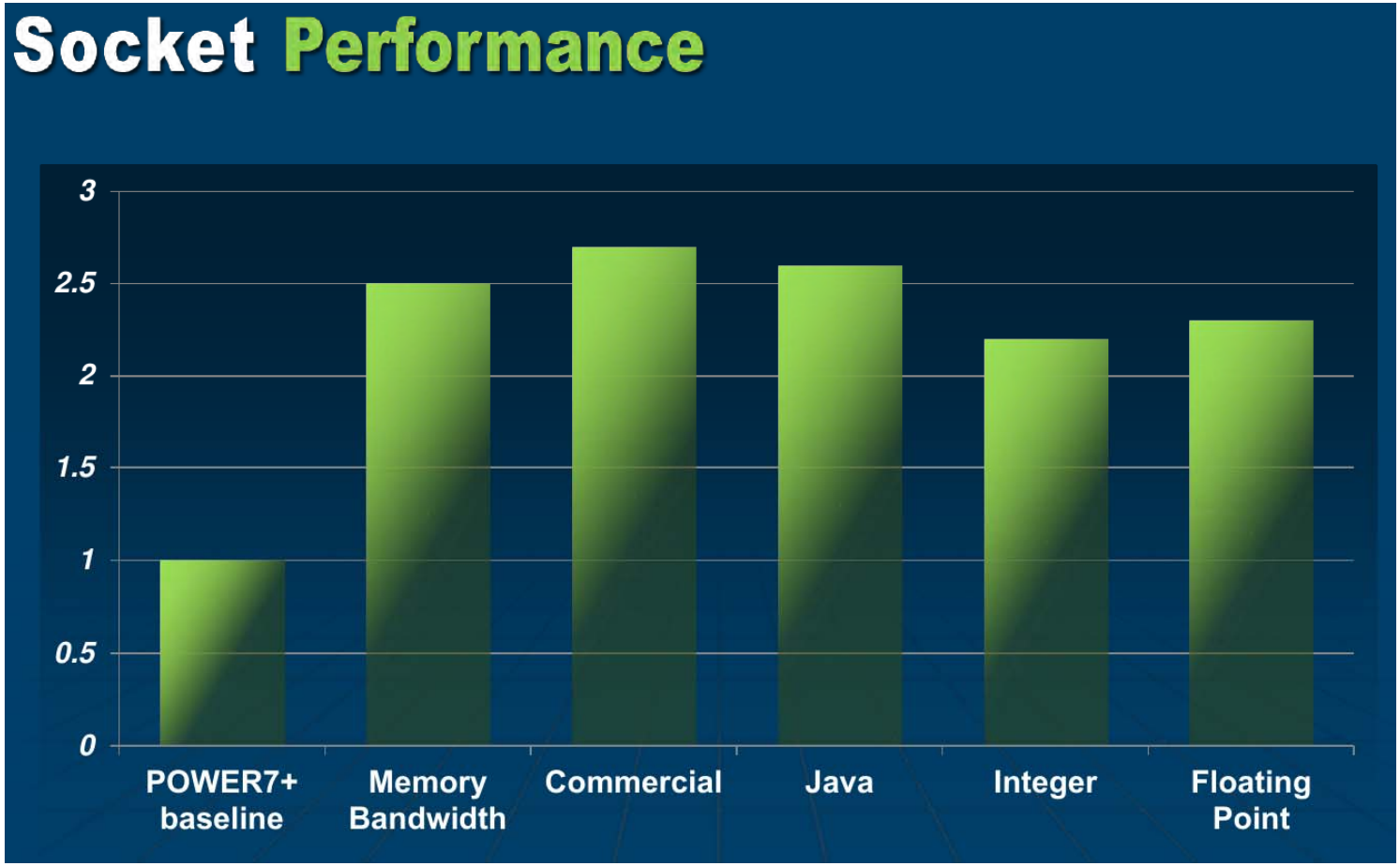


http://www.hwsw.hu/kepek/hirek/2014/05/p8_spec1.jpg

POWER8 vs POWER7

- 2-3x faster
- CAPI
- Bigger caches and off-chip caching
- More cores and more threads
- Adds Centaur memory interconnects for higher memory bandwidth

POWER8 vs POWER7+



http://www.computerbase.de/forum/attachment.php?attachmentid=361164&d=1377627118

POWER vs PowerPC (Architecture)

- PowerPC is a modified version of POWER, with incompatibilities
  - PowerPC has some additional instructions
  - More restrictions on reserved fields in instructions
  - Different behaviour with reserved bits in registers
  - Others

POWER vs PowerPC (Target)

- PowerPC is basically a consumer version of POWER

POWER vs x86 Architecture

- Few differences in terms of general performance
- POWER is much better at virtualization
- POWER is better at data transaction processing and data analytics

Future of POWER8

- Expected to clock up to 5GHz over lifespan.
- Provide open-source alternative to x86.
- Overtake x86 as a more modern, more powerful platform.

Sources

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Questions?